Logsys Spartan 6

# Simple I/O Controller Register Map V.1.0[1]

## *Register summary*

| | | | |
|---|---|---|---|
| BASE+0x00 | 8 bit | RW | LED |
| BASE+0x01 | 8 bit | RW | DISP1 |
| BASE+0x02 | 8 bit | RW | DISP2 |
| BASE+0x04 | 16 bit | RW | GPIO_DATA |
| BASE+0x06 | 8 bit | R | DIPSWITCH |
| BASE+0x08 | 16 bit | RW | GPIO_DIR |
| BASE+0x0A | 8 bit | R | NAV_BTN |
| BASE+0x0C | 8 bit | RW | IE (Interrupt Enable) |
| BASE+0x0D | 8 bit | R/W1C | IF (Interrupt Flag) |

**Please note that 8 bit register allow only 8 bit WRITE access!**
**Please note that 16 bit register allow only 16 bit WRITE access!**

| | Bits 31..24 | Bits 23..16 | Bits 15..8 | Bits 7..0 |
|---|---|---|---|---|
| BASE+0x00 | - | DISP2 (RW) | DISP1 (RW) | LED (RW) |
| BASE+0x04 | - | DIPSWITCH(R) | GPIO_DATA (RW) | |
| BASE+0x08 | - | NAV_BTN(R) | GPIO_DIR (RW) | |
| BASE+0x0C | - | | IF(R/W1C) | IE(RW) |

## *Detailed description*

| | | | |
|---|---|---|---|
| BASE+0x00 | 8 bit | RW | LED |

LED register is designed to control the 8 LEDs through the CPLD.

| | | | |
|---|---|---|---|
| BASE+0x01 | 8 bit | RW | DISP1 |

DISP1 register is designed to control the right seven segment display through the CPLD.

| | | | |
|---|---|---|---|
| BASE+0x02 | 8 bit | RW | DISP2 |

DISP1 register is designed to control the left seven segment display through the CPLD.

| | | | |
|---|---|---|---|
| BASE+0x04 | 16 bit | RW | GPIO_DATA |

Peripheral contains a variable with (C_GPIO_WIDTH = default 13) general purpose I/O peripheral, which is optionally synthesized into the core if C_GPIO_ENABLE =1.
If peripheral is not selected for synthesis read access to this register returns zero.

- *Writing* to this register sets the output value bit-by-bit basis, if the corresponding GPIO_DIR bit is zero (output mode).
- *Reading* this register allows to read the input pin bit-by-bit basis.

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| | | | |
|---|---|---|---|
| BASE+0x08 | 16 bit | RW | GPIO_DIR |

Peripheral contains a variable with (C_GPIO_WIDTH = default 13) general purpose I/O peripheral, which is optionally synthesized into the core if C_GPIO_ENABLE =1.
If peripheral is not selected for synthesis read access to this register returns zero.

Direction of the GPIO peripheral is set bit-by-bit basis.

- Logic 0 – Output
- Logic 1 – Input

The register default value is 1 (input) on each used bit position.

| | | | |
|---|---|---|---|
| BASE+0x06 | 8 bit | R | DIPSWITCH |

DIPSWITCH register is designed to read the status of the 8 DIP Switches through the CPLD.

| | | | |
|---|---|---|---|
| BASE+0x0A | 8 bit | R | NAV_BTN |

Bit 0: Navigation Up
Bit 1: Navigation Down
Bit 2: Navigation Left
Bit 3: Navigation Right
Bit 4: Navigation Button

Bit 5: Btn 0
Bit 6: Btn 1
Bit 7: Btn 2

| | | | |
|---|---|---|---|
| BASE+0x0C | 8 bit | RW | IE (Interrupt Enable) |

Interrupt sources can be enabled bit-by-bit basis.

Bit 0: DIP SWITCH change interrupt
Bit 1: NAVIGATION Switch change interrupt
Bit 2: BUTTON change interrupt
Bit 3: GPIO change interrupt

Bit 7..4: Not used, read as 0

| | | | |
|---|---|---|---|
| BASE+0x0D | 8 bit | RW | IF (Interrupt Flag) |

Interrupt flag register.

Each bit defines an interrupt event described in IE register. (Read access). If the corresponding IE bit is not set, the event is not causing interrupt to the processor, although the register can be polled

**1 should be written to IF register to acknowledge the corresponding interrupt.**